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A DESIGN FOR A 32-CHANNEL MULTIPLEXER.(U)
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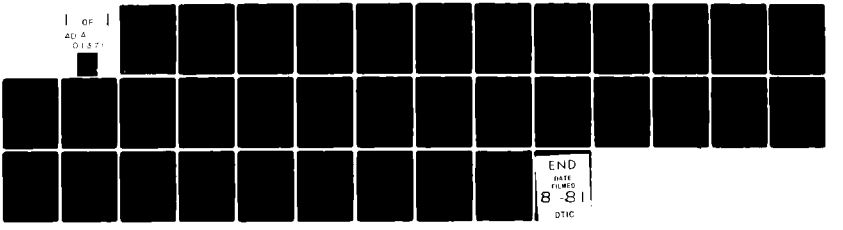

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ROYAL AIRCRAFT ESTABLISHMENT

A DESIGN FOR A 32-CHANNEL MULTIPLEXER

by

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SUMMARY

A multiplexer was required for the recording of data during flight trials of unmanned aircraft (UMA) navigation sensors. This Memorandum gives details of the design and a summary of the tests carried out to evaluate the performance.

LIST OF CONTENTS

1 INTRODUCTION

RN2 Division has been involved in the development of a variety of sensors intended mainly for unmanned aircraft (UMA) navigation systems. In general, the design and development of the sensors was carried out extramurally and the prototype systems were flight tested by RAE in manned aircraft. As the sensors were designed for relatively slow moving vehicles the testing was performed using a Wessex helicopter.

The characteristics of the sensors were such that the signals varied from raw data of several kHz bandwidth to processed data and test signals of only a few Hz bandwidth. It was also necessary to record aircraft attitude, heading and height, and synchronising signals from a camera and a kinetheodolite tracking system.

A 7-track instrument tape recorder had been used in previous trials; this was now inadequate, however, since in addition to the basic data, there could be up to 30 other signals monitoring the system simultaneously. For this reason, it was necessary to use some form of multiplexing system to condense as much information as possible before recording.

The design described in this Memorandum is based on a simple analogue system. Much of the constraint placed on the design was due to the tape recorder, so brief descriptions of its performance and operation have been included where necessary.

2 CHOICE OF MULTIPLEXER DESIGN

To keep the multiplexer's bandwidth requirement within the recorder's range, only the low frequency signals could be multiplexed. Pitch, roll, height and most of the test signals were of low frequency, but the raw data and kinetheodolite signals required the full bandwidth of the recorder.

At the time, a digital multiplexer was available from another part of the UMA programme. This converted analogue inputs to digital words, each channel being assigned an 8-bit word. This design was not chosen for the following reasons:

(a) The 8-bit analogue-to-digital conversion with a resolution of 1/255 was considered marginal.

(b) The digital system only catered for single polarity signals. A multiplexer capable of passing both positive and negative levels was required for the recording of pitch and roll signals.

(c) The multiplexer was originally intended for use in a telemetry system and was considered rather too complex for the problem in hand.

(d) Rather than try to modify the system to be compatible with the requirements, it seemed safer to design a simple but reliable analogue system from scratch, hence allowing the designer complete control over its operating characteristics.

An analogue sampling switch was chosen as the basis for the design, each input channel being scanned for a short time and the voltage level recorded on tape, thus building up a sequence of snap-shots. The demultiplexer would reconstitute the signals by sampling the sequence.

MOSFET analogue switches were available in integrated circuit form. Each integrated circuit contained eight MOSFET switches and the gating control could be derived directly from TTL outputs. The essence of the following design is, therefore, a sequenced control of 32 such switches.

3 DESIGN CONSTRAINTS

3.1 Recording format

Each of the seven recorder channels had two modes of recording, 'Direct Record' (DR) and 'Frequency Modulated' (FM). An improvement in signal-to-noise ratio is gained by using FM because it is not susceptible to the amplitude modulating noise associated with magnetic tapes. Although dc and low frequencies can be recorded with FM, there is the disadvantage of a small bandwidth compared with the DR mode at the same tape speed. For example, a speed of $7\frac{1}{2}$ in/s gives bandwidths of 0-5 kHz and 100 Hz to 40 kHz for the FM and DR modes respectively.

The FM mode requires filters to remove unwanted carrier signal during playback of a recording. Two types were available:

(i) A Bessel response filter which has no overshoot to step inputs.

(ii) A Tchebychef response filter which is more efficient in removing the carrier but suffers some overshoot when fast switching edges are encountered.

The Bessel type is recommended for use with fast rise time signals.

3.2 Bandwidth requirement

A tape speed of $7\frac{1}{2}$ in/s had previously been chosen on the basis of raw data bandwidth requrements. Since the multiplexer would require the use of an FM channel, to preserve the dc content of the analogue samples, the available recording bandwidth was a nominal 5 kHz, setting an upper limit for the multiplexer sampling rate.

It was found that a 1ms sample pulse could be recorded satisfactorily at the above tape speed. Although fast edges were lost, the recorded pulse still contained a flat top, showing that the output had reached a steady state. A flat top pulse was essential since the demultiplexer had to reconstitute the sampled signal by sampling the pulse. Any major distortion of the pulse would result in non-linear gain errors in the recovered signal. As mentioned earlier, the Bessel filter gave the best response to the pulse, but even so the overshoot of the Tchebychef response filter was contained within the first half of the pulse, leaving the second half available for the demultiplexer to sample.

The 1ms sample pulse required a 1kHz clock to drive the gate control of the analogue switches. Since there were 32 channels to be sampled, each channel would be sampled once every 32 ms, giving a channel sample rate of just over 30 Hz. This set the bandwidth for each of the multiplexer channels. The Nyquist-Shannon sampling theorem would allow a bandwidth of 15 Hz, half the sampling rate, in the ideal case, but for practical purposes 10 Hz was taken as a safe upper limit. This was adequate for the sensor trials.

3.3 Input level range

The tape recorder had eight input level ranges that could be selected. The smallest range catered for a voltage swing from -0.1 V to + 0.1 V and the largest for a swing from -20 V to +20 V.

The analogue switches could take voltages between two bias levels V_{DD}, a positive value, and V_{EE} a negative value. The maximum safe value of $(V_{DD} - V_{EE})$ was quoted by the manufacturer as 15 V. Since all the signals that required multiplexing lay within the range ±5 V, this same range was chosen for the multiplexer. This gave a value of 10 V for $(V_{DD} - V_{EE})$ and used the full dynamic range of the recorder with its ±5V peak input setting.

The design of the switches was such that V_{DD} was also logic level high for the gate control. Since TTL was to be used without additional buffering, V_{DD} could not be set greater than +5 V, thus placing another constraint on the input range.

3.4 Output level range

The output range of the recorder had been set to ±1 V. For convenience, the entire system, ie the multiplexer, recorder and demultiplexer, was given unity gain. This meant that the demultiplexer required a gain of 5.

3.5 Offset error monitoring

Since the FM mode allows for the recording of dc signals, offset voltage errors and drifts can be introduced into the system by the recorder. To highlight these the multiplexer was designed to allow a OV reference to be applied to the input of all channels simultaneously. Offsets occurring within the multiplexer and demultiplexer would also show up.

3.6 Power supplies

The multiplexer was designed to work from the aircraft's 28V dc supply. Small scale, low power dc to dc converters were available to produce dual polarity supplies for operational amplifiers. The demultiplexer was designed to operate from 230 V mains.

3.7 Mechanical features

As the multiplexer would be installed in aircraft a standard $\frac{1}{2}$ ATR box was used to house the circuits. Special cables were made up to connect the 32 signal sources to the multiplexer. These allowed BNC connectors to be used at the sources whilst using a compact multi-way cannon connector at the multiplexer.

4 SYSTEM DESIGN

4.1 The multiplexer operation

Fig 1 shows a schematic diagram of the multiplexer. The 32 inputs are buffered and multiplexed in groups of eight onto four lines. These four are then multiplexed onto one and this signal passes through the output buffer to the recorder. No input filtering has been provided, since it was assumed that the input signals would already have been band limited. Also, no input limiting has been provided as this would:

(i) increase the complexity and component count of the circuits,

(ii) introduce non-linearity to signals near the extremes of the input range.

In addition, it was assumed that the signals were externally limited.

Fig 2 shows the input stage in more detail. Switch S1 comprises the contacts of a relay. With S1 open, the input signal appears at the input of the amplifier, $R_2 \gg R_1$. With S1 closed, reference 0 V is applied to the input and any offset voltages occurring in the multiplexer, recorder and demultiplexer can be monitored. R1 acts as a dummy load for the input signal source when the relay contacts are closed. It was assumed that the input signal sources would have very low output impedances, R1 being chosen as 1 kΩ.

R3 was included to limit the current to the MOSFET switches in the event of an input over voltage. Though this protects the ICs to some extent, the data in other channels can become corrupted by the excessive current flowing into the switch substrate.

A diagram of the timing and control circuit for the analogue switches is shown in Fig 3. The clock has a period of 1 ms and is used to increment the counter, the outputs of which constitute the gate control for the MOSFET switches. Each of the buffered inputs in Fig 1 is routed through to the recorder in turn for 1 ms, and a particular channel is scanned once every 32 ms.

The clock (CK) is used by the demultiplexer for synchronisation and the preset signal (PR) is used to identify the scan of channel 32. Since this signal appears once every 32 ms the playback of a recording can be started anywhere and the demultiplexer will lock on to the correct sequence of channels within this time. The clock and preset pulses are mixed and recorded on a separate tape track from the data. A separate track was used for the timing in order to keep the design simple and immune to tape speed variations.

The sketch in Fig 4 shows typical waveforms that would appear at the data and clock outputs of the multiplexer. For complete circuit diagrams refer to Figs 5 to 11.

4.2 The demultiplexer operation

Fig 12 shows a sketch of the demultiplexer's timing circuits. The recorded timing waveform passes through the high-pass filter to remove any dc offset introduced by the recorder. Amplifiers 1 and 2 then separate the clock and preset signals. The Schmitt NAND gates provide fast edges for the TTL counter and sample pulse generator.

On each positive going clock edge the counter is incremented by one unit and the logic demultiplexer selects a route from the output of the pulse generator to one of the sample and hold ICs shown in Fig 13. On each negative clock edge the monstable produces a nominal 100μs pulse, which puts the selected sample and hold in the sample mode for this short time. It can be seen from the waveforms in Fig 4 that the demultiplexer samples in the middle of the channel scans.

Fig 13 shows the sample and hold circuits and their associated output smoothing filters. Amplifier 3 is used to set the gain of the system, nominally times five. The gain can be adjusted to suit other requirements. The offset adjustment is used primarily to zero the amplifier rather than remove recorded offsets. The lowpass filters are of a second-order Butterworth design and have a cutoff frequency of 10 Hz. Circuit diagrams have been included in Figs 14 and 15.

5 SYSTEM PERFORMANCE

The measurements in sections 5.1 to 5.6 were obtained using a RACAL STORE 7 DC tape recorder, and unless stated otherwise all measurements were performed with a tape speed of 7½ in/s. Section 5.7 was included for a comparison of the performance of the multiplexing system without the recorder. Leading particulars for the multiplexer and demultiplexer have been included in the Appendix.

5.1 Gain

The gain of the system was set to unity at dc, so that a 5V input at the multiplexer gave a 5V output at the demultiplexer. The gain will change with frequency because of the sampling action and the smoothing filters and a measured response is given in Fig 16. For signals above 6 Hz the output was very distorted and so the results are only approximate above this frequency.

5.2 Linearity

With the gain of the system already set to unity the output of a channel was monitored over the full input range; Fig 17 shows the result graphically. Although the output remains linear beyond the specified ±5 V range, it is not a good idea to deliberately use it so; voltages above the bias levels of the analogue switches can cause excessive current to flow into their common substrate, affecting other channels. It was found that the input on any channel could swing between +5.5 V and -6.0 V without corrupting another channel. The reason why a slightly larger negative swing can be tolerated is that the negative bias used is -5.6 V.

5.3 Phase

The filters and sampling action introduce phase delays between channels carrying different frequencies. The filters have the phase response of a second-order Butterworth filter with low-pass cutoff at 10 Hz. The sampler introduces the linear phase response

$$\phi(\omega) = \omega T/2 \text{ radians},$$

where ω is the angular frequency of the signal and T is the sampling period.

The phase difference between the output of the demultiplexer and input to the multiplexer was measured over the frequency range 0.1-8 Hz and the results have been plotted in Fig 18.

For these measurements the tape was stopped and the recorder used in the bypass mode, in which the input signals bypass the recording heads and appear at the output directly. This mode of operation is convenient for such measurements as the tape motion only introduces an additional lag that will be common to all channels.

Another source of phase delay is the sequential sampling nature of the multiplexer. The effect of this is not noticed on low frequency signals, within the system bandwidth, due to the smoothing of the filters. However, anomalous effects will occur when switching type signals are multiplexed. For example, two inputs that switch simultaneously at the input will appear to switch in sequence at the output. The delay between them will depend on the channel separation.

5.4 Noise

To study the noise level of the system a OV reference signal was applied to a channel and the demultiplexed output monitored on an oscilloscope. It was found that apart from some power supply mains ripple, of about 2 mV peak-to-peak, the noise was of a low frequency, so an X-Y plotter was used to obtain the hard copy shown in Fig 19.

The low-frequency noise was caused mainly by the demultiplexer sampling the output noise of the recorder, the bulk of this being residual FM carrier signal having a nominal frequency of 20 kHz. Therefore, the best performance was obtained by using the Tchebychef output filters on the recorder as they gave the greatest carrier attenuation. Fig 19 was produced using this type of filter.

Another source of low-frequency noise is tape recorder wow and flutter, caused by irregular tape motion over the heads. The effect of this on the recorder's output is shown in Fig 20 for a OV input. It will be magnified by the demultiplexer.

Low-frequency noise causes the greatest problem because it cannot easily be removed from the low-frequency signals required. In view of this attempts were made to reduce the noise at source by providing additional filtering of the recorder's outputs. As well as filtering the data channel, the timing signals were also passed through a similar filter to preserve the relative phase of the two waveforms. Third-order, low-pass filters were used with a cutoff frequency of 5 kHz, this being the lowest frequency that could be used, with this order filter, without distorting the waveform.

Though the carrier noise was greatly reduced, other noise of a lower frequency became more prominent at the output of the recorder. This could possibly have been caused by harmonics of the sampling rate. As a result no visible improvement on the system noise level was gained by the additional filtering. Lack of time prevented any more complicated attempts at reducing the noise level and Fig 20 is representative of the system in its present state.

5.5 Offset errors

Offset voltage errors are introduced mainly by the recorder. Unfortunately they drift considerably during the first hour of operation of the STORE 7 DS, and the effect is magnified five times by the demultiplexer gain.

The error drift of the system was monitored at the output of the demultiplexer with 0 V applied to the multiplexer input. Fig 21 shows the result with the recorder operating in the bypass mode. The source of the offset and drift was later traced to the replay filters of the FM channels.

5.6 Crosstalk

Crosstalk is a measure of the interaction between signals in different channels of the multiplexer system. It was found that the recorder introduced crosstalk by biassing the data channel waveform with an offset proportional to the mean level of the waveform. This caused level shifts to occur in all channels and the amount depended on the number of active channels and the size of the signals they carried.

To obtain a quantitative measure of the crosstalk, one channel was given a 0 V reference and its output monitored while other channels were given peak positive and negative dc signals. A peak positive signal in one channel caused a negative 6-8mV shift in the reference channel. A peak negative signal gave the same bias level but positive. When two channels were active the bias was twice as much and increased consistently as more channels became active.

A detailed study of the recorder electronics indicated that the source of the bias lay within the design of the output filters, and is probably unique to this make of recorder.

As a short cut to overcome the problem for the flight trials, one of the spare multiplexer channels was grounded continuously. During playback its output was used to monitor the bias.

5.7 Performance independent of the recorder

This section has been included to illustrate the performance of the multiplexer system without the recorder. To do this the multiplexer was coupled to the demultiplexer with 5:1 attenuators to provide the correct levels. Three features were studied: the noise, the offset drift and crosstalk, which had all been attributed to the inclusion of the recorder.

(a) Noise

Fig 22 is a time scan of the demultiplexer output produced in the same way as Fig 19. The peak noise is shown to be only a few millivolts and was caused by the sampling action mixing with residual mains noise. Several attempts were made to improve the situation by heavier screening and earthing; however, it seemed that the presence of the mains noise was a limitation of the ±15V power supply used in the demultiplexer.

(b) Offset drift

The offset drift was monitored, as in Fig 21, from switch on up to a period of 2 h. No measurable offset drift was detected.

(c) Crosstalk

The effect mentioned in 5.6 did not occur and no other sources of crosstalk were apparent above the noise.

5.8 Potential use with a digital system

In view of the above-mentioned performance, it would be possible to interface the multiplexer with an analogue-to-digital converter and record in a digital format. About 12 bits would be required of the A/D converter to make use of the full range of the multiplexer, so it would be necessary to use the DR recording format. A D/A converter would be used before the demultiplexer. This would overcome the noise, offset drift and crosstalk errors introduced by the recorder, and the performance would be governed by the A/D interfacing.

It would also be logical to integrate the clock and synchronisation pulses into the digital data stream and hence create a single line system.

CONCLUDING COMMENTS

The design of the multiplexer was a simple analogue system and its performance was sufficient for the sensor trials. The main sources of noise and drift in the system proved to be in the recorder and not a feature of the multiplexer. Although it was designed to be compatible with a RACAL STORE 7 DS tape recorder, it should operate with any other multi-track recorder having an FM recording format on at least two tracks. The design contains the basic features for any multiplexing system, analogue or digital, and thus it could be made an integral part of a digital telemetry system, say.

Appendix

LEADING PARTICULARS

Multiplexer

Input range:	±5 V
Maximum input frequency:	10 Hz
Impedence:	1 MΩ nominal, relays open 1 kΩ nominal, relays closed
Output range:	Clock channel ±5V logic levels Data channel ±5 V
Clock frequency:	1 kHz
Supply:	25V dc at 1 A (relays active)
Weight:	3 kg approximately

Demultiplexer

Input range:	Clock channel ±1V logic levels Data channel ±1 V
[illegible]:	Clock channel 40 kΩ nominal Data channel 100 kΩ nominal
[illegible]:	Variable from ±2 V to ±10 V Preset to ±5 V
[illegible]:	230V mains at 100 mA

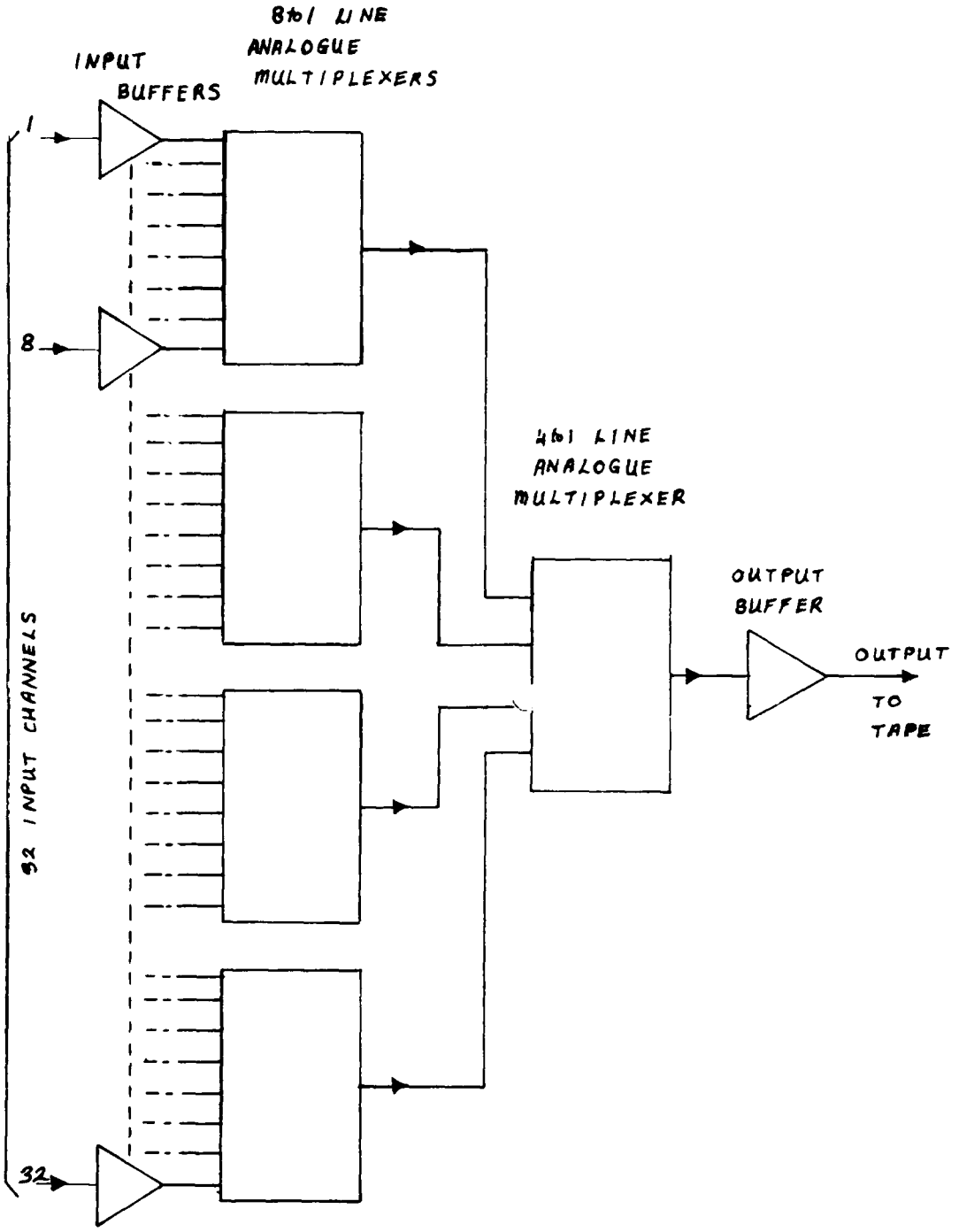


Fig 1 Block diagram of multiplexer data channel

Fig 2

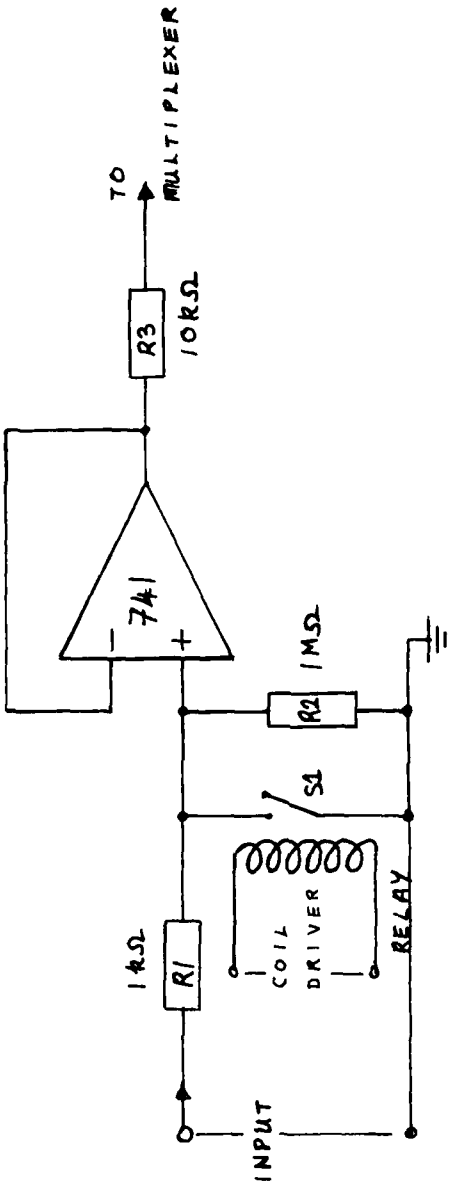


Fig 2 Detail of input buffer stage

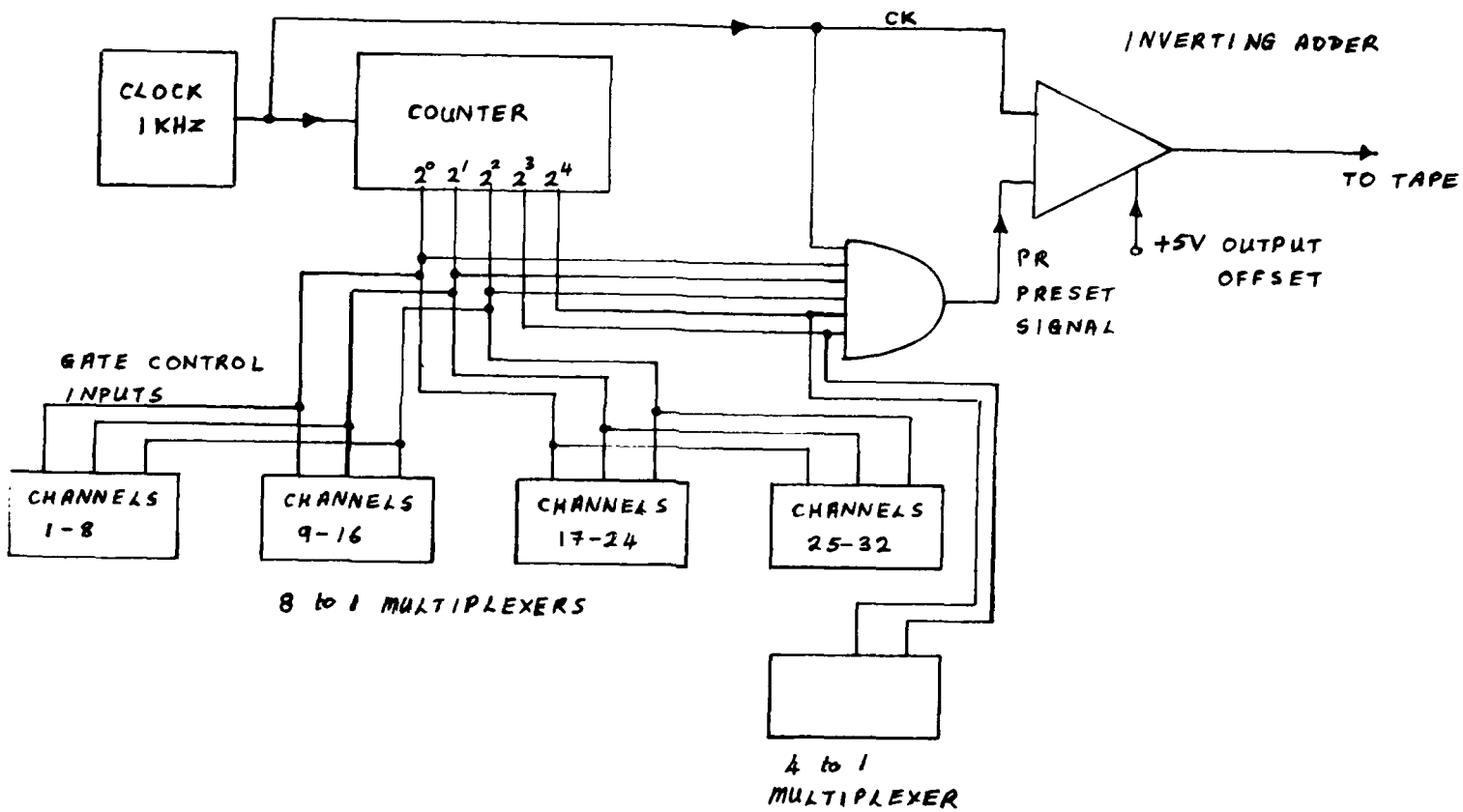


Fig 3 Block diagram of multiplexer timing and control circuit

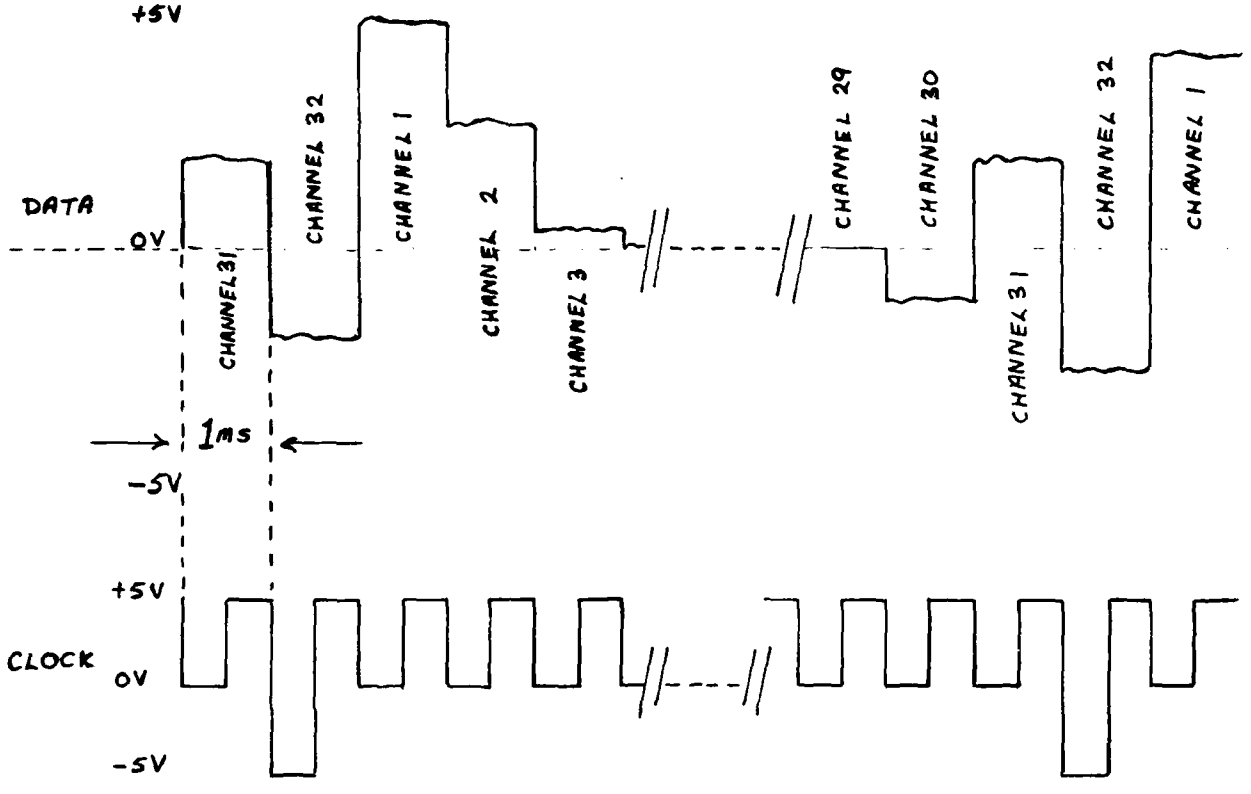


Fig 4 Sketch of typical data and timing waveforms

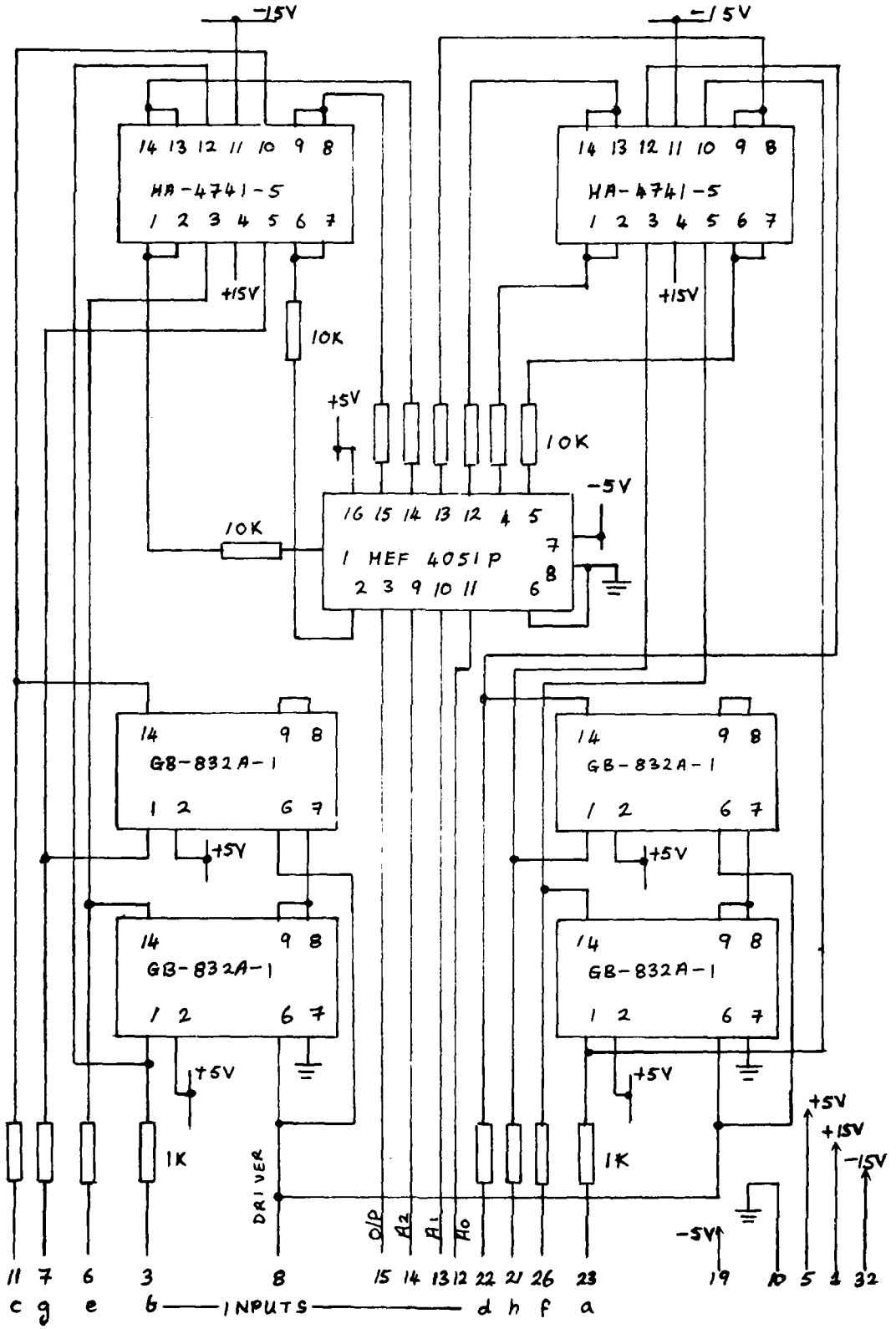


Fig 5 Input buffer, 8-1 multiplexer board

Fig 6

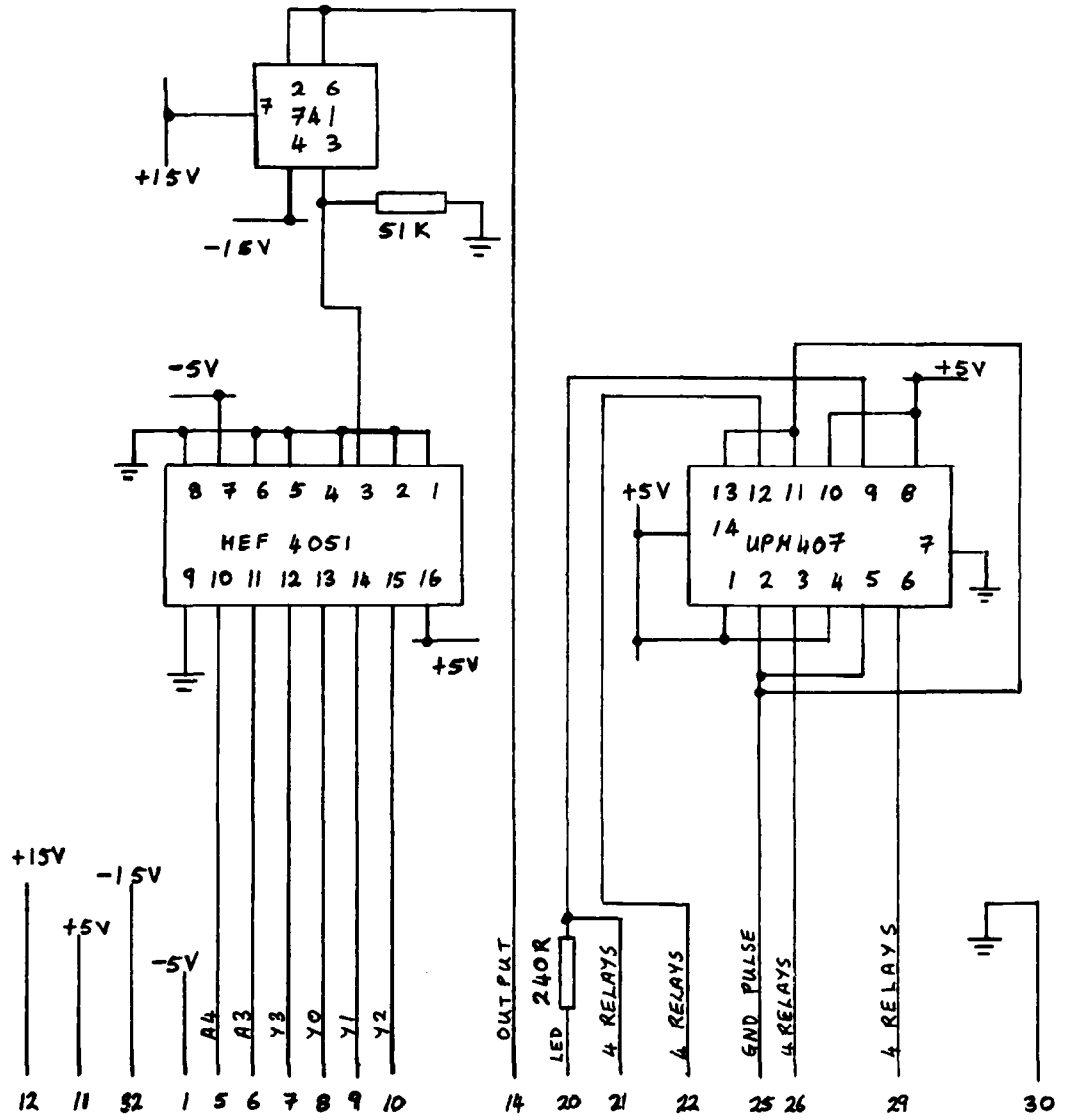


Fig 6 4-1 multiplexer, O/P buffer, relay drivers

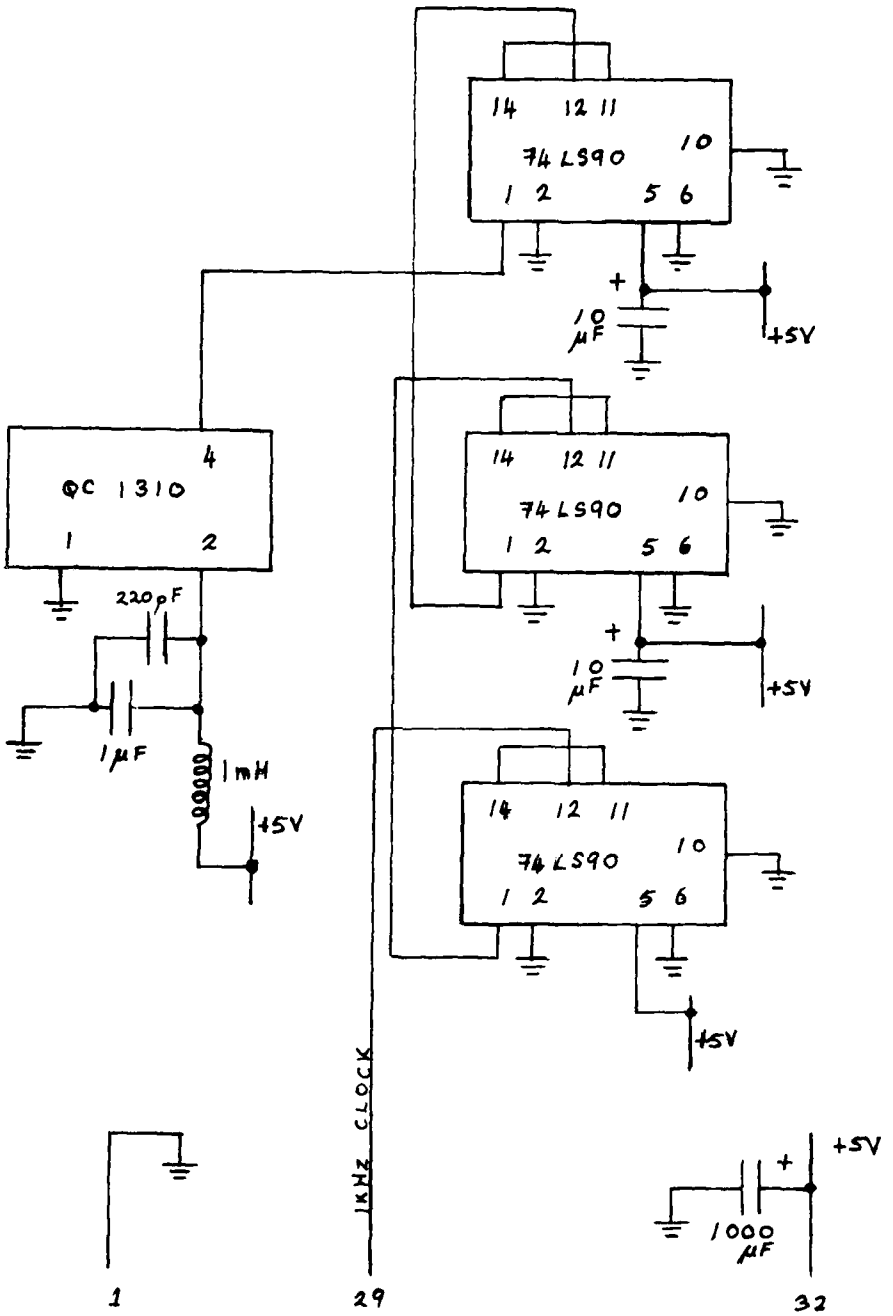


Fig 7 1kHz clock board

Fig 8

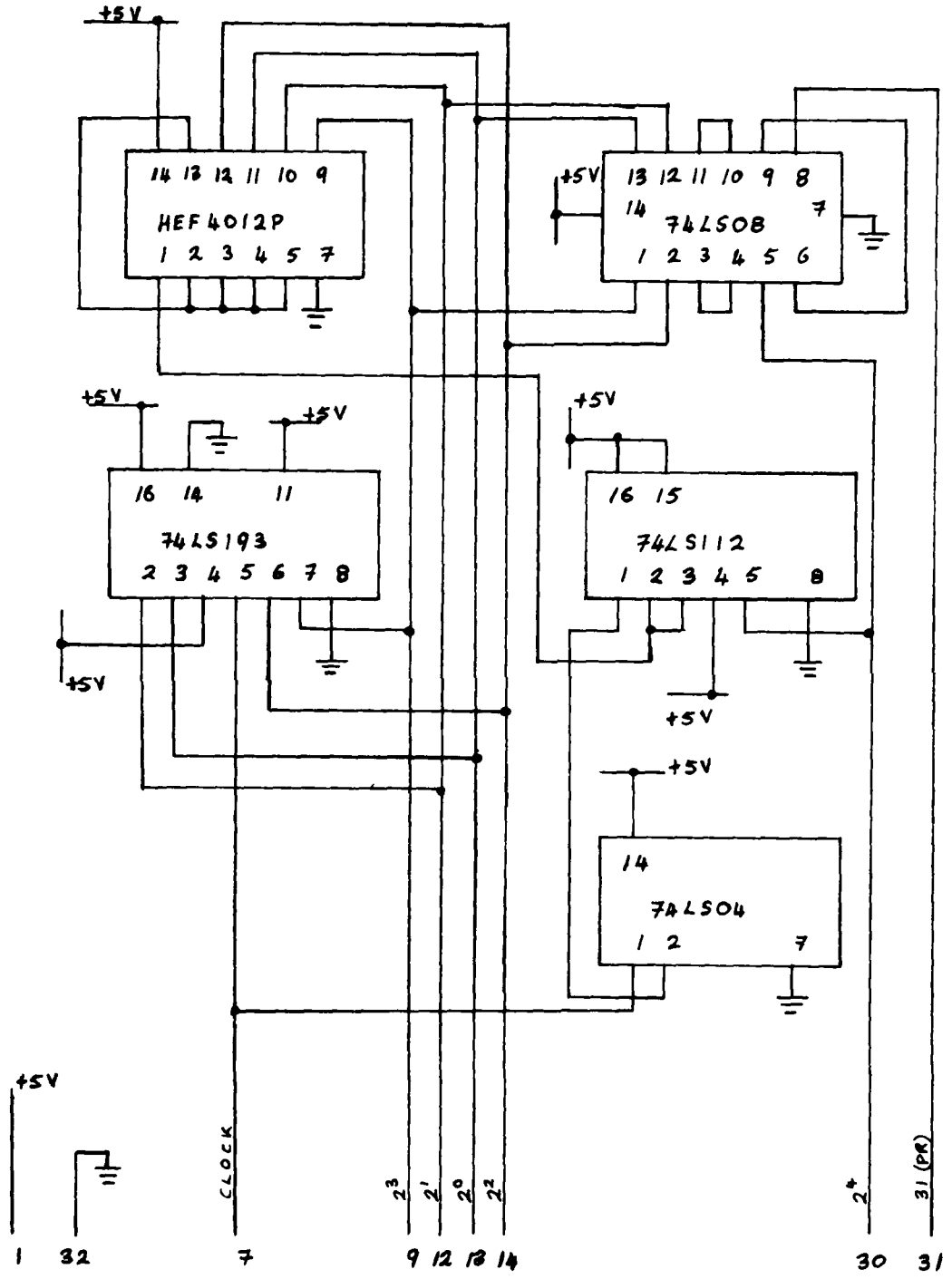


Fig 8 Multiplexer control counter

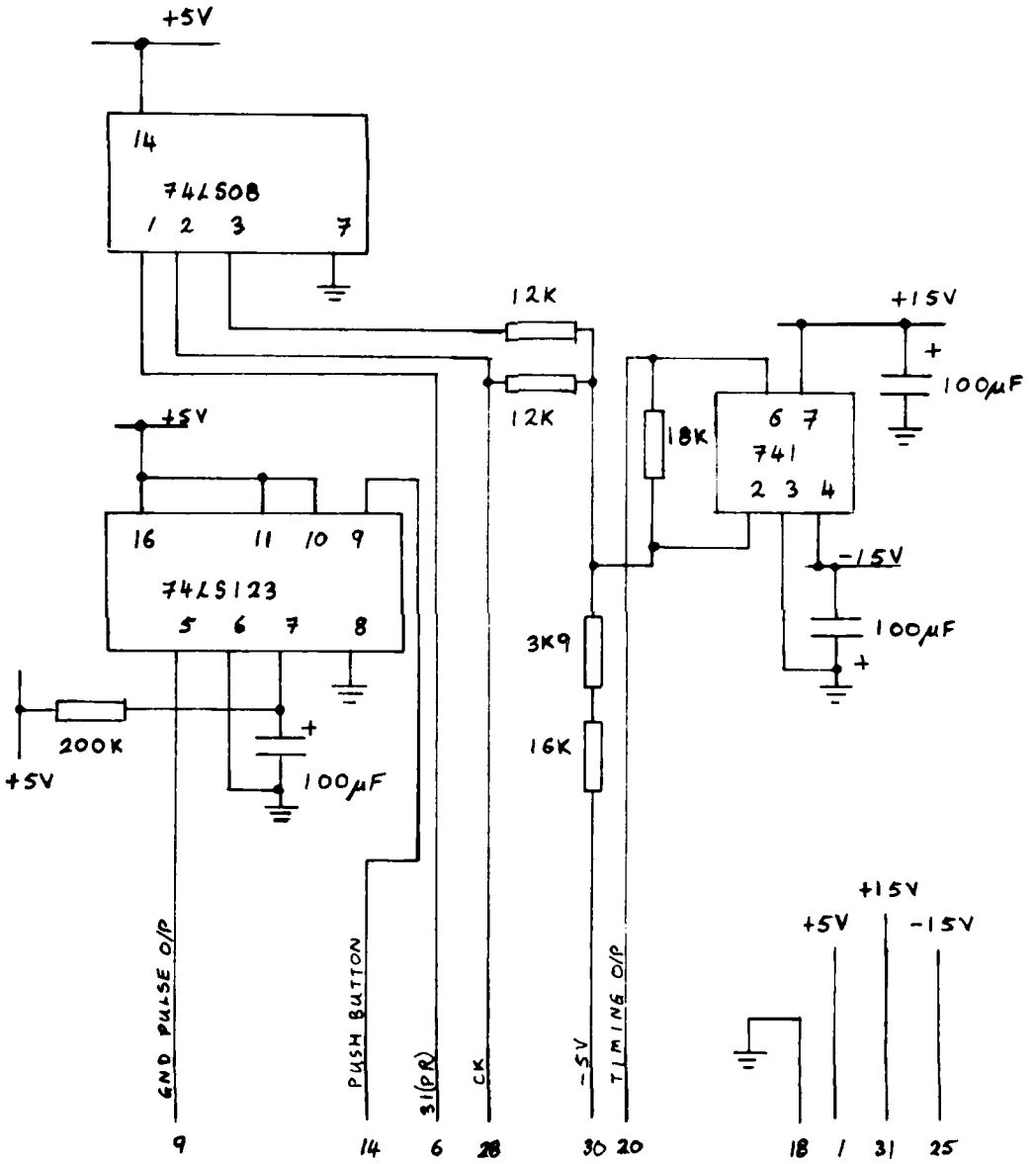
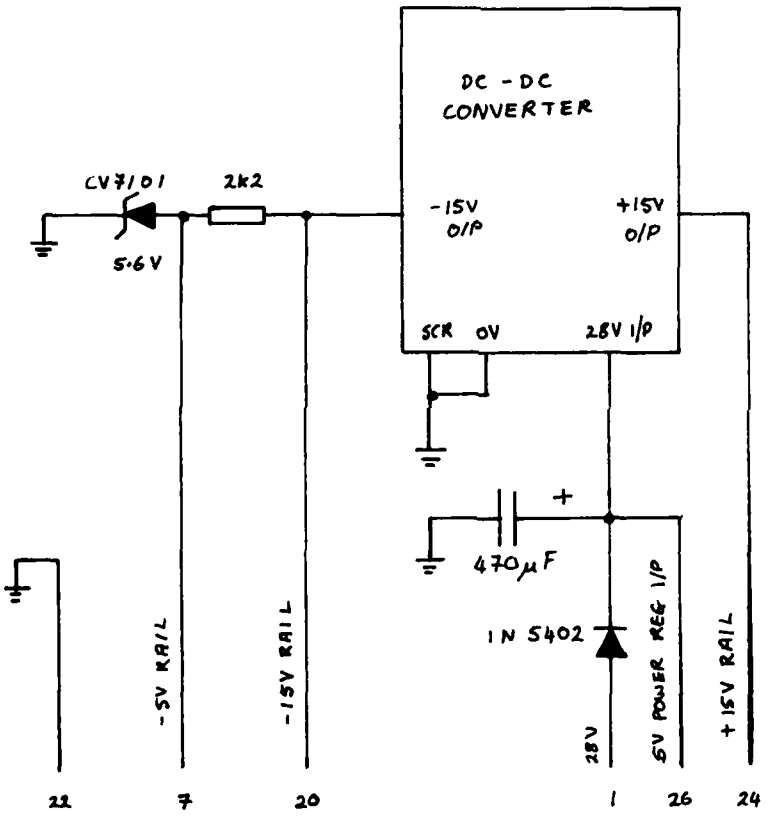


Fig 9 Timing waveform O/P circuit, relay pulse circuit

Fig 10


DC - DC
CONVERTER
CV7101
2k2
5·6V
-15V
O/P
+15V
O/P
SCR
0V
28V I/P
470μF
1N 5402
-5V RAIL
-15V RAIL
28V
5V POWER REG I/P
+15V RAIL
22
7
20
1
26
24

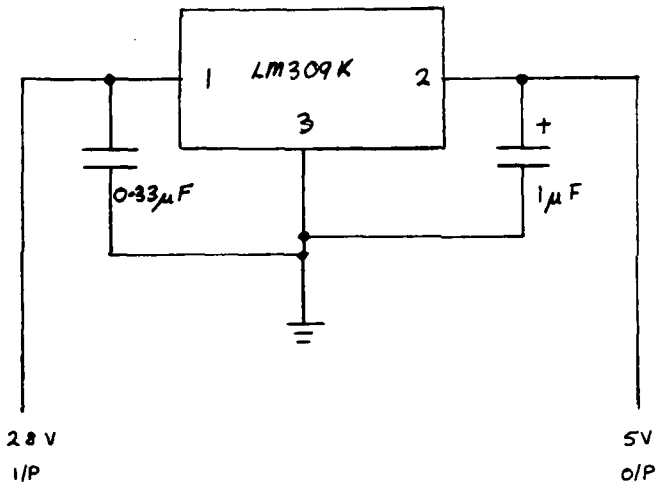


Fig 11 +5V power supply

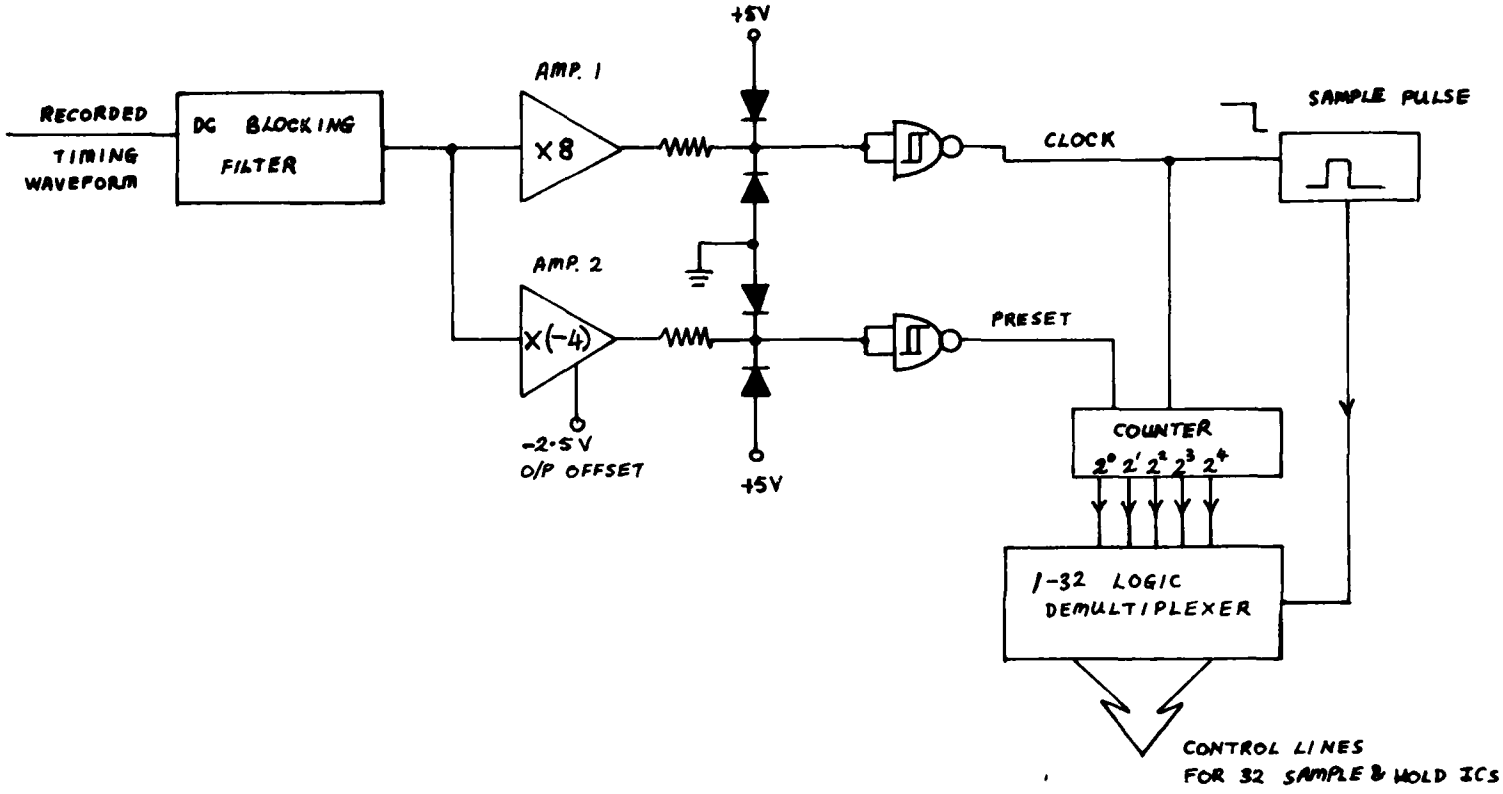


Fig 12 Block diagram of demultiplexer timing circuit

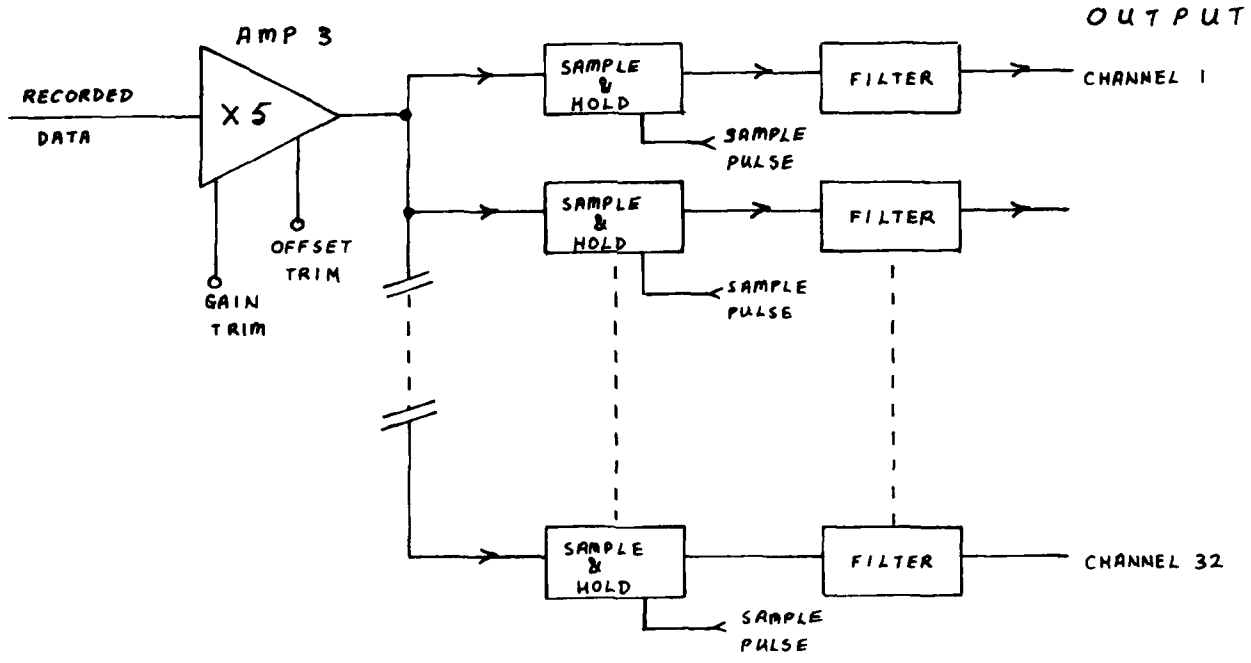


Fig 13 Block diagram of demultiplexer data circuit

Fig 14

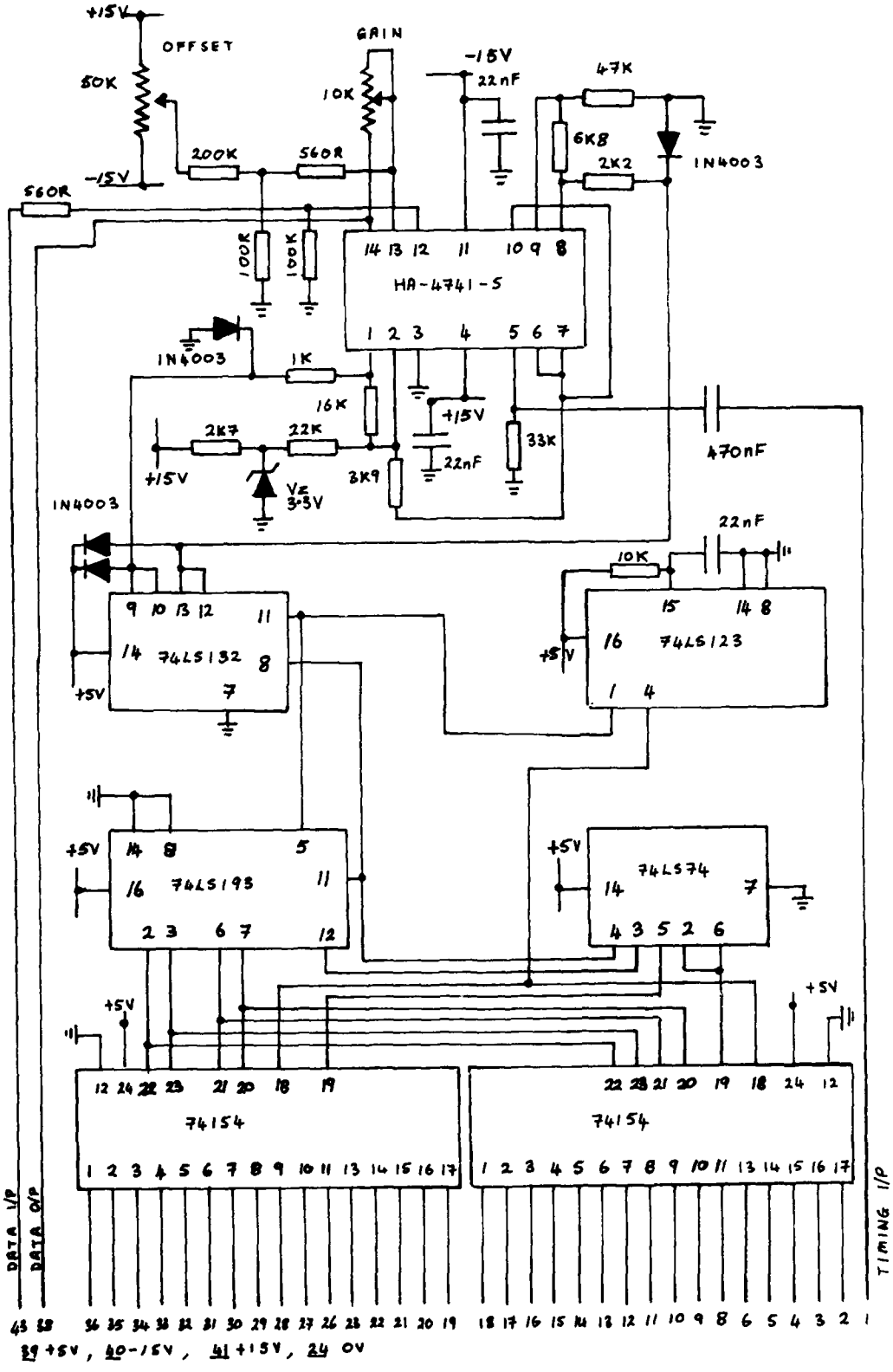


Fig 14 Demultiplexer input board

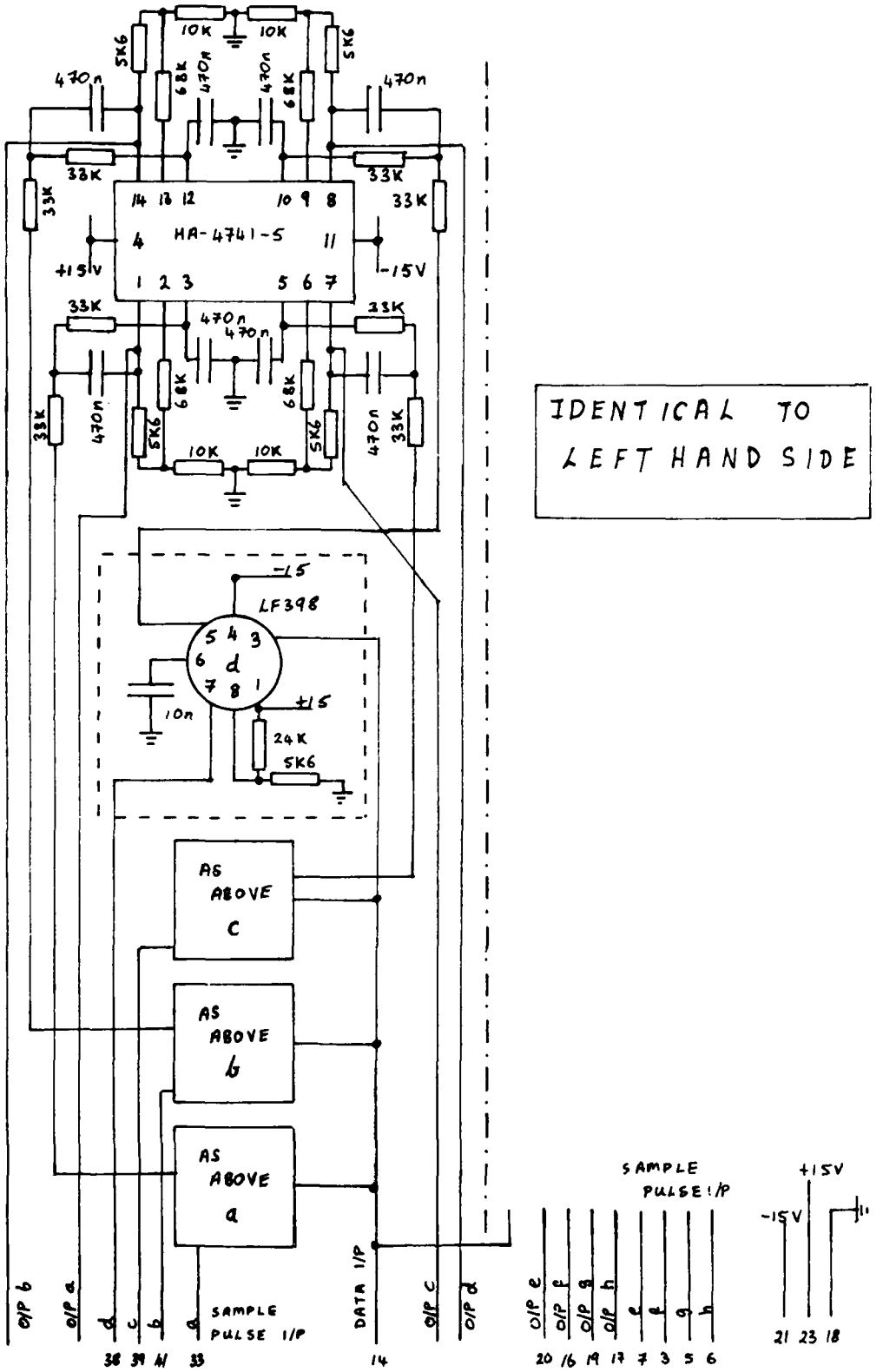


Fig 15 Demultiplexer output board

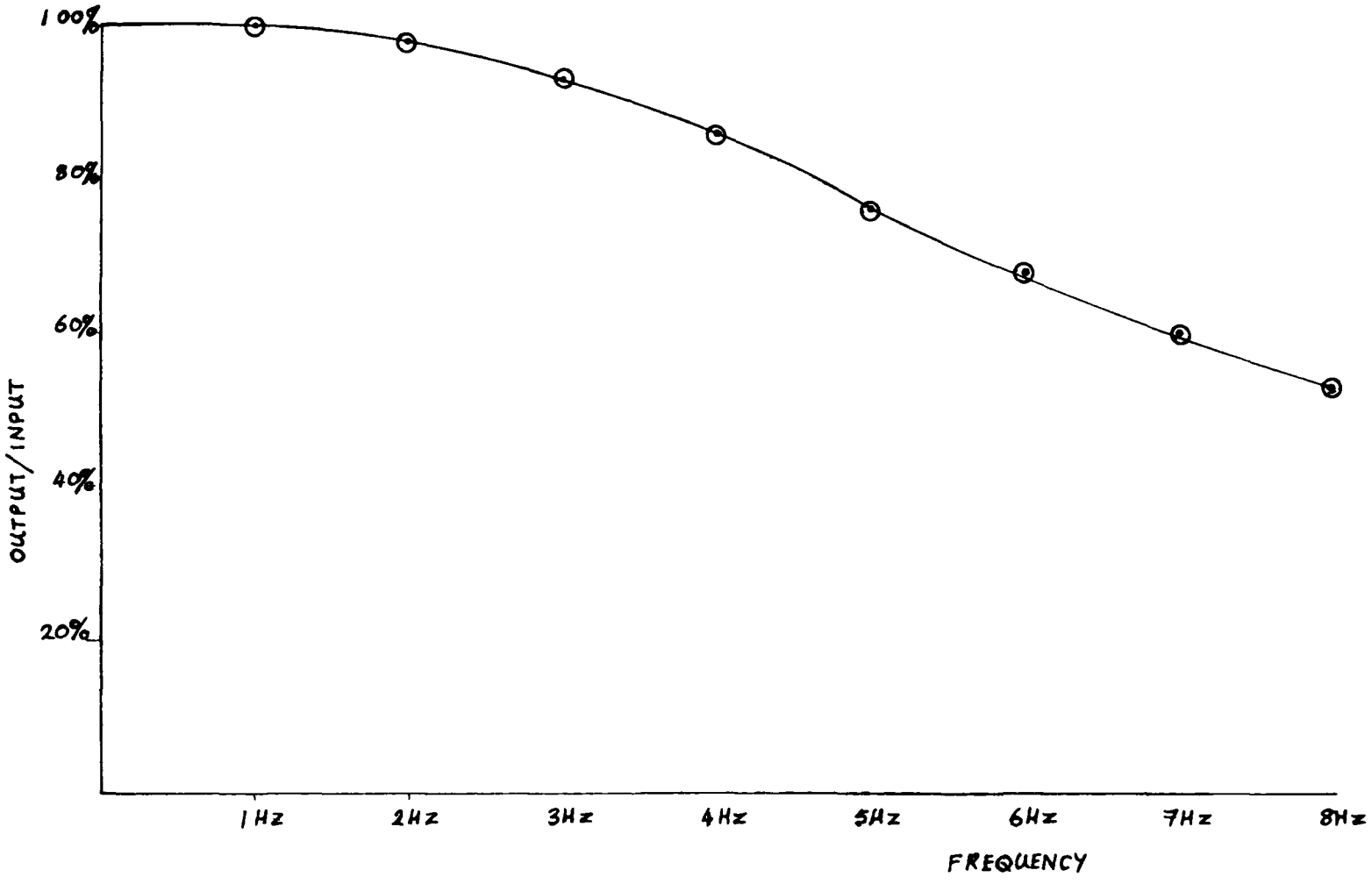


Fig 16 System gain frequency response

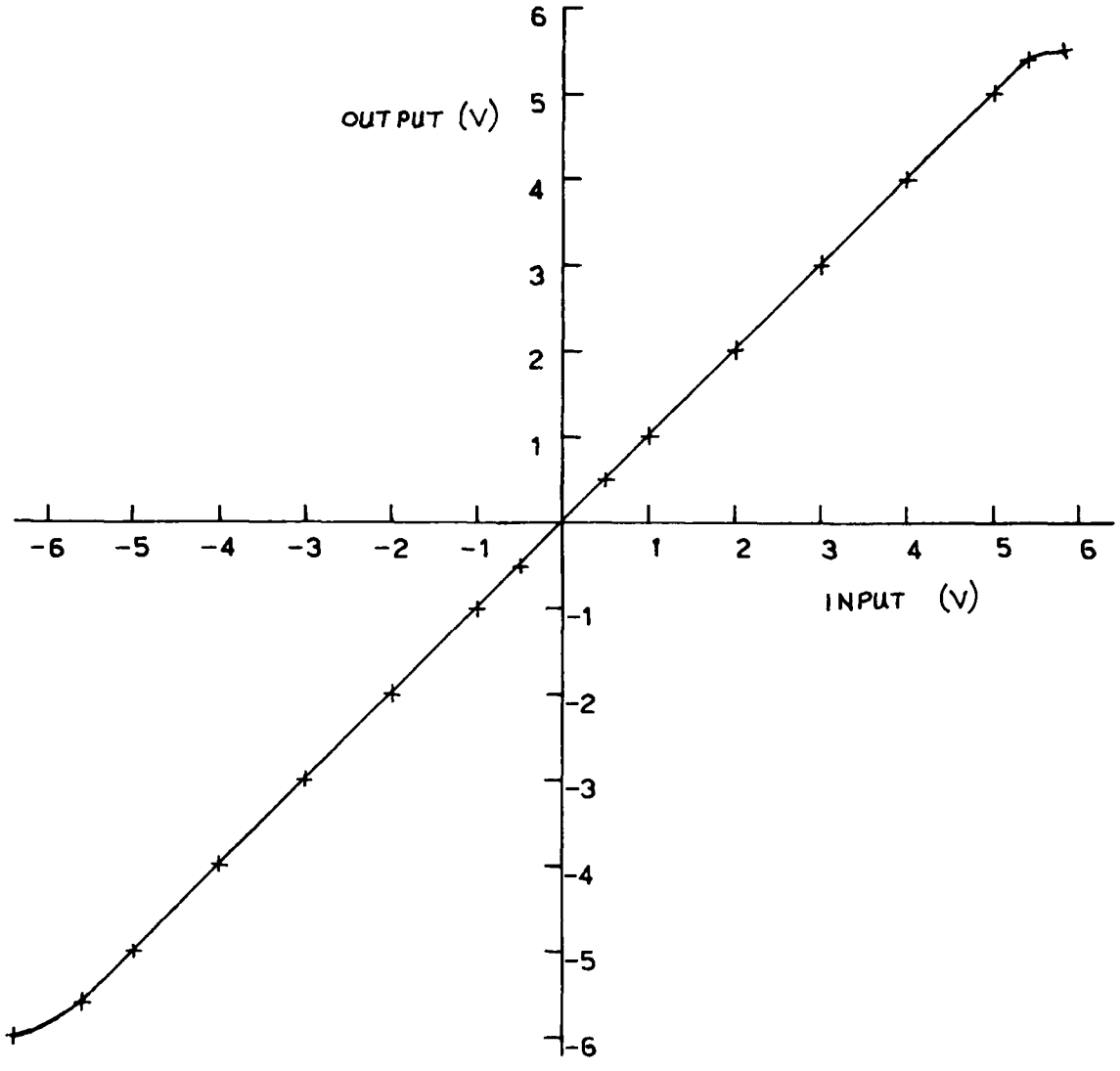


Fig 17 System linearity

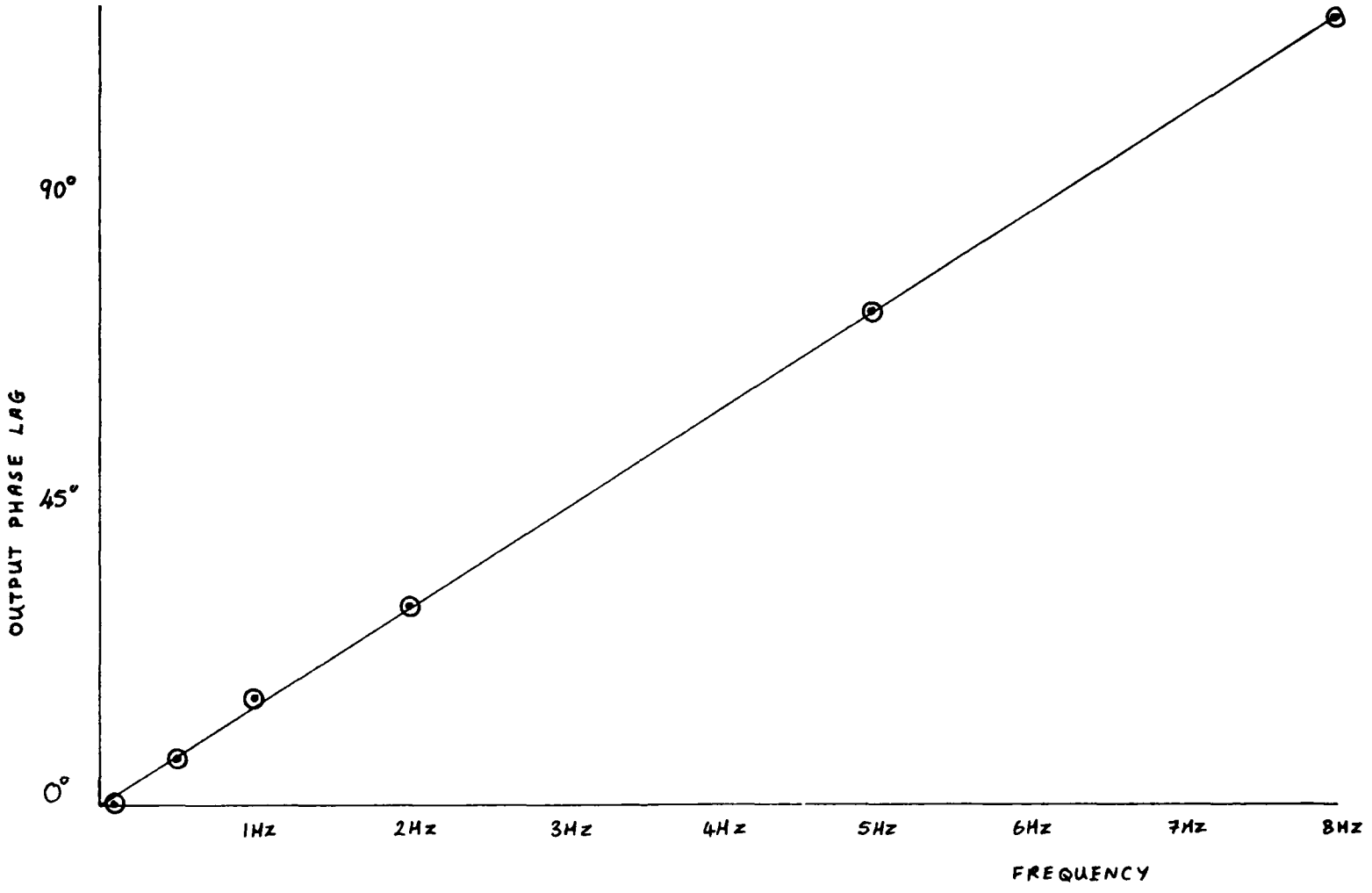


Fig 18 System phase frequency response

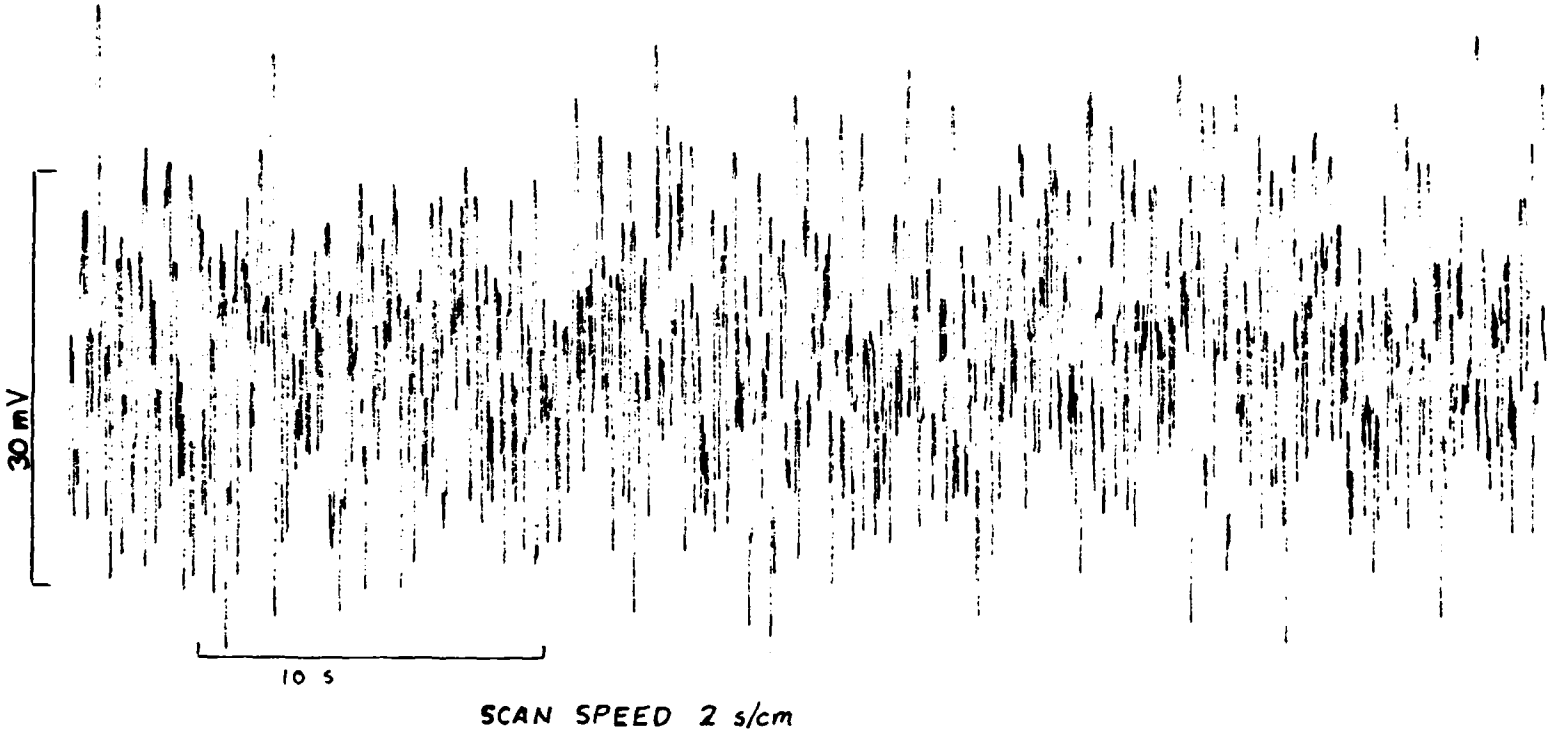


Fig 19 Output noise with 0 V input

Fig 19

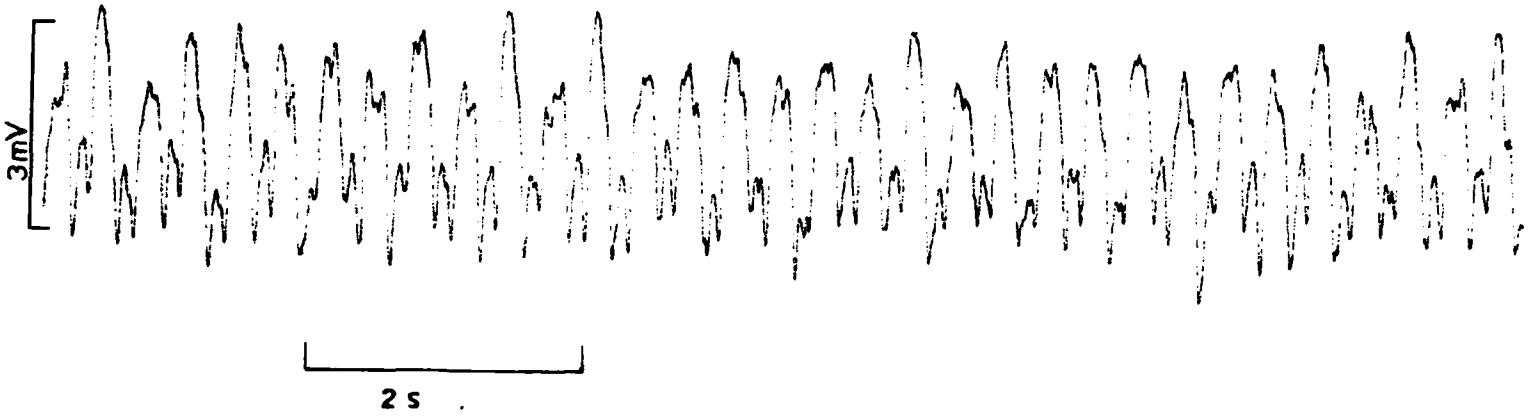


Fig 20 Effect of wow and flutter on recorder O/P with 0 V I/P

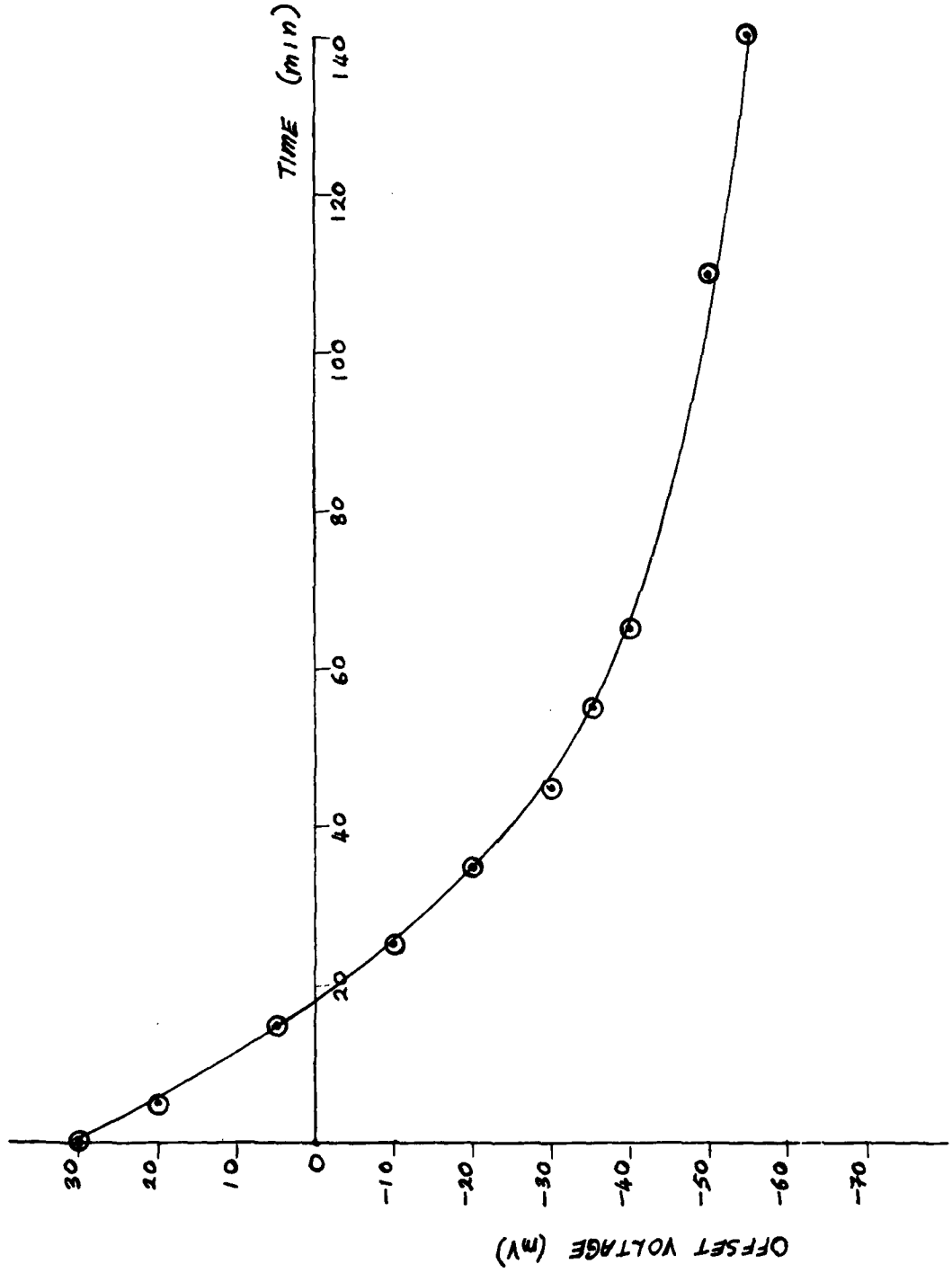


Fig 21 Offset voltage drift including recorder for 0 V input

Fig 22

Fig 22 Output noise with 0 V input excluding recorder

REPORT DOCUMENTATION PAGE

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17. Abstract

A multiplexer was required for the recording of data during flight trials of unmanned aircraft (UMA) navigation sensors. This Memorandum gives details of the design and a summary of the tests carried out to evaluate the performance.


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